

In the Specification:

Please replace paragraph [0043] with the following amended paragraph:

[0043] The source 2 includes a shallow source extension 2a and a deep source portion 2b in a source-drain region. The drain 4 includes a shallow drain extension 4a and a deep drain portion 4b in the source-drain region. The source-drain region is in the substrate 5 under the gate 3. The source-drain region extends lengthwise to include the source 3 and the drain 4. The source-drain region has a shallow source-drain region between the source extension 2a and the drain extension 4a. The source-drain region has a deep source-drain region between the deep source portion ~~[[3a]]~~ **2b** and the deep drain portion ~~[[4a]]~~ **4b**. For example, the semiconductor device 1 is a field effect transistor, FET. An FET comprises either a PMOSFET, a p-type metal oxide silicon field effect transistor, or an NMOSFET, an n-type metal oxide silicon field effect transistor.

Please replace paragraph [0044] with the following amended paragraph:

[0044] The semiconductor device 1 has a source depletion region 6. The source depletion region 6 includes a shallow source depletion region 6a and a deep source depletion region 6b. The semiconductor device 1 has a drain depletion region 7. The drain depletion region 7 includes a shallow drain depletion region 7a and a deep drain depletion region 7b. The source-drain depletion region is between the source ~~[[3]]~~ **2** and the drain 4. The source-drain depletion region is in the substrate 5 under the gate 3, and is where the SCE or punch through effect can occur.

Please replace paragraph [0048] with the following amended paragraph:

[0048] Fig. 3 discloses another embodiment of the present invention that is indicated as **Sd, in which a deep-pocket ion implant 8 and a shallow-pocket ion implant 9 are provided in staggered configuration.** ~~With reference to Fig. 3, the~~ **The** deep-pocket ion implant 8 is at the drain side, and in the drain depletion region 7. The shallow pocket **ion** implant 9 is at the source

side, and in the source depletion region 6. As shown in Fig. 3, the semiconductor device 1 has only one of each of the deep-pocket ion implant 8 and the shallow-pocket ion implant 9.

Please replace paragraph [0049] with the following amended paragraph:

[0049] Fig. 4 discloses another embodiment in which a deep-pocket ion implant 8 and a shallow-pocket ion implant 9 are provided in a staggered configuration that is indicated as sD in Fig. 4. ~~With reference to Fig. 4, In this embodiment,~~ the deep pocket ion implant 8 is at the source side, and in the source depletion region 6. The shallow-pocket ion implant 9 is at the drain side, and in the drain depletion region 7. As shown in Fig. 4, the semiconductor device 1 has only one of each of the deep-pocket ion implant 8 and the shallow-pocket ion implant 9.

Please replace paragraph [0062] with the following amended paragraph:

[0062] With continued reference, to Fig. 9, a process step of rapid thermal annealing of the semiconductor device 1 is performed, to refine the crystalline structure and repair structural damage caused by ion implantation. Annealing causes joining of the source extension 2a and the deep source 2**b**. Annealing further causes joining of the drain extension 4a and the deep drain 4**b**.

Please replace paragraph [0064] with the following amended paragraph:

[0064] Fig. 11 discloses a deep pocket primary implant 8 formed by performing the process step of Fig. 6, with a tilt angle tilted to the source side of the semiconductor device 1. Fig. 11 discloses a deep pocket secondary implant 8**8** that is countered by ion implants to be further disclosed by Fig. 15.

Please replace paragraph [0065] with the following amended paragraph:

[0065] Fig. 12 discloses a drain side, shallow pocket primary implant 9 and a shallow pocket secondary implant 99 formed by performing the process step of Fig. 6, by having the tilt angle tilted toward the drain side of the semiconductor device 1. The primary implant 9 is under the gate 3.

Please replace paragraph [0068] with the following amended paragraph:

[0068] Fig. 15 discloses a deep source portion 2b and a deep drain portion 4b formed by the process step disclosed by Fig. 9. In Fig. 15, the source side, deep-pocket primary implant 8 and the drain side, shallow-pocket primary implant 9 become asymmetric ion implants in staggered configuration, respectively, when the deep-pocket secondary implant 88 and the shallow-pocket secondary implant 99 are counterdoped. Then a process of rapid thermal annealing of the semiconductor device 1 is performed as disclosed by Fig. 9.

Please replace paragraph [0070] with the following amended paragraph:

[0070] Fig. 17 discloses a drain side, deep pocket primary implant 8 formed by performing the process step of Fig. 6, with a tilt angle tilted to the drain side of the semiconductor device 1. Fig. 17 discloses a deep pocket secondary implant 88 that is counterdoped by ion implants to be disclosed by Fig. 21.

Please replace paragraph [0071] with the following amended paragraph:

[0071] Fig. 18 discloses a source side, shallow-pocket primary implant 9 and a drain side, shallow-pocket secondary implant 99 formed by performing the process step of Fig. 6, with the tilt angle tilted toward the source side of the semiconductor device 1. The primary implant 9 is under the gate 3 at the source side of the semiconductor device 1.

Please replace paragraph [0074] with the following amended paragraph:

[0074] Fig. 21 discloses a deep source portion 2b and a deep drain portion 4b formed by the process disclosed by Fig. 9. In Fig. 21, the drain side, deep primary implant 8 and the source side, shallow primary implant 9 become asymmetric ion implants, respectively, when the **deep-pocket** secondary implant 88 and the **shallow-pocket** secondary implant 99 are countered. Then a process of rapid thermal annealing of the semiconductor device 1 is performed as disclosed by Fig. 9.

Please replace paragraph [0076] with the following amended paragraph:

[0076] Fig. 23 discloses a drain side, deep pocket primary implant 8 formed by performing the process step of Fig. 6, with a tilt angle tilted to the drain side of the semiconductor device 1. Fig. 23 discloses a deep pocket secondary implant 88 that is countered by ion implants to be disclosed by Fig. 27.

Please replace paragraph [0077] with the following amended paragraph:

[0077] Fig. 24 discloses a drain side, shallow pocket primary implant 9 and a shallow pocket secondary implant 99 formed by performing the process step of Fig. 6, by having the tilt angle tilted toward the drain side of the semiconductor device 1. The drain side, primary implant 9 is under the gate 3 at the drain side of the semiconductor device 1.

Please replace paragraph [0080] with the following amended paragraph:

[0080] Fig. 27 discloses a deep source portion 2b and a deep drain portion 4b formed by the process disclosed by Fig. 9. In Fig. 27, the drain side primary deep implant 8 and the drain side primary shallow implant 9 become asymmetric ion implants, respectively, when the **deep-pocket** secondary implant 88 and the **shallow-pocket** secondary implant 99 are countered. Then a

process of rapid thermal annealing of the semiconductor device 1 is performed, as disclosed by Fig. 9.

Please replace paragraph [0082] with the following amended paragraph:

[0082] Fig. 29 discloses a source side, deep pocket primary implant 8 formed by performing the process step of Fig. 6, with a tilt angle tilted to the source side of the semiconductor device 1. Fig. 29 discloses a deep pocket secondary implant 88 that is countered by ion implants to be disclosed by Fig. 33.

Please replace paragraph [0083] with the following amended paragraph:

[0083] Fig. 30 discloses a source side, shallow pocket primary implant 9 and a shallow pocket secondary implant 99 formed by performing the process step of Fig. 6, by having the tilt angle tilted toward the source side of the semiconductor device 1. The source side, primary implant 8 is under the gate 3 at the source side of the semiconductor device 1.

Please replace paragraph [0086] with the following amended paragraph:

[0086] Fig. 33 discloses a deep source portion 2b and a deep drain portion 4b formed by the process disclosed by Fig. 9. In Fig. 33, the source side, deep primary implant 8 and the source side, shallow primary implant 9 become asymmetric ion implants, respectively, when the deep-pocket secondary implant 88 and the shallow-pocket secondary implant 99 are countered. Then a process of rapid thermal annealing of the semiconductor device 1 is performed as disclosed by Fig. 9.

Corrections to Drawings and Submission of Formal Drawings:

The following corrections to the drawings have been made to correct the typographical errors with several of the reference numerals in the originally filed drawing figures:

FIGs. 11 – 15; 17 – 21; 23 – 27; 29 – 33: The reference number designating the deep pocket secondary implant is changed from 8 to 88. (See also the corresponding amendment to the Specification.)

FIGs. 12 – 15, 18 – 21; 24 – 27; 30 – 33: The reference number designating the shallow pocket secondary implant is changed from 9 to 99. (See also the corresponding amendment to the Specification.)

Four (4) sheets of Annotated Marked-Up Drawings are attached to this paper. A set of formal drawings incorporating the corrected figures are submitted herewith for the examiner's approval. The formal drawings consist of nineteen (19) sheets containing FIGs. 1-36.